Single Bit 6T SRAM for Better SNM and Reduced Power Consumption

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***Abstract*— the major focus of this paper is to stress on reduction of power dissipation and improvement in SNM for a 6T single bitline SRAM cell. A new 6T SRAM design is presented with a reduction of 55.17% in power consumption and SNM improvement by 4.53% having same on chip area is presented in this work.**

I. Introduction

Memories are an integral part of most of the digital devices and hence reducing power consumption of memories is very important to improve system performance, efficiency, and reliability. A conventional 6T SRAM cell has two cross coupled inverters with two bit lines and a word line to hold a data bit as long as the power supply is ON. Power consumed during the operation phase is primarily categorized into two-Active and Leakage Power. Active power is the power consumed when both pull-up and pull-down networks are active, creating a direct current path from V_{dd} to ground. Leakage power is the power consumed when charges leak through a transistor that is in OFF state. Power dissipation can be decreased by 3 ways: 1) Lowering the frequency. 2) Reducing V_{swing}. 3) Reducing the bit-line capacitance.

Static Noise Margin SNM is the maximum amount of voltage noise that can be introduced at the output of the two inverters such that the cell retains its data. It is the side of the biggest square that can be embedded into the butterfly curve [1]. Higher the SNM, more stable will be the circuit.

II. Proposed Design

The proposed 6T SRAM cell uses a single bitline BL and an additional RL to control M3 which is connected to ground. The aspect ratio for nMOS is 2 and pMOS is 3. BL is also connected to the drain of M2. Since a single bitline is used, capacitance is reduced as compared to conventional designs. SRAM cell has three operational modes-read, write and hold.

- ***Write:*** For Writing 0, BL is discharged through the circuit keeping RL and WL high. For writing 1 BL is pre-charged to V_{dd}, WL is high so high voltage enters into the internal latch.
- ***Read:*** SRAM cell requesting the data from the internal latch termed as 'read'. BL is pre-charged to V_{dd} and RL is high. To read 0, if M2 is ON that shows Q' is 1. Thus cell reads 0 which is the data at Q. While reading 1, BL should not be discharged through M2 which implies Q' is 0 and data at Q is 1.
- ***Hold:*** SRAM cell is used to store the data in steady state condition. WL is 0, the access transistor M6 is OFF and the value inside the latch is independent on BL.

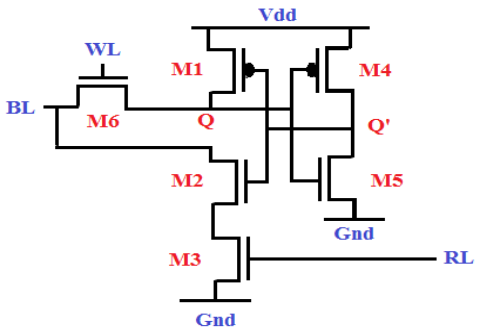

Figure 1. Proposed Single Bit 6T SRAM

III. Results

The simulation is done in Microwind 3.5 in 90nm technology. Results shown in Fig. 2, have been simulated for 10ns with step size of 0.1ps. The results have been compared with the Design-I [2] and Design-II [3] and the comparison is shown in Table I.

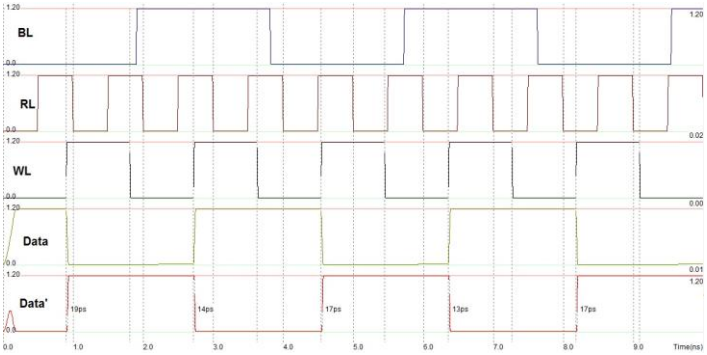

Figure 2. Result for Proposed 6T SRAM

TABLE I. Comparison of Power Consumption, Area and SNM

Designs	Power (µW)	Area (µm^2)	SNM (mV)
Design-I	5.728	5.04	274.57
Design-II	5.735	5.52	276.92
Proposed	2.571	5.40	294.84

IV. Conclusion

The new proposed designed for the 6T SRAM cell with single bit line shows improvement in power dissipation by 55.17%, and SNM is improved by 4.53% without any adverse effect on area.

References

[1] A. Pavlov and M. Sachdev, *"CMOS SRAM Circuit Design and Parametric Test in Nano-Scaled Technologies," Springer S.B.M. B.V.*, pp. 1–202, Nov. 2008.

[2] Saurabh and P. Srivastava, "Low Power 6T- SRAM", *ICEE-2012, pp 1-4*, Dec. 2012.

[3] V. M. C. Wang, "Low Power Dual Word Line 6-Transistor SRAMs", WCECS 2009, Vol. 1, Oct. 2009.